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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/695,624	TOHSCHE, ULF	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5,9-11 and 15-20* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/13/05 has been entered.

2. Note that, in this office action, the indicated allowability of claims 5, 8-11 and 15-20 in the last office action is withdrawn in view of the newly discovered reference(s) as discussed in the rejections below.

Claim Objections

3. Claims 6-9, 11 and 15-20 are objected to because of the following informalities:

Claim 6, line 1, "an inverted version of" should be deleted and should be moved to after "having" on line 3, i.e., after having on line 3, --an inverted version of-- should be inserted.

Claims 7 and 9 are objected to because they include the informality of claim 6.

Also in claim 9, line 2, "upon activation" is suggested to be changed to --in response to an active state-- since a signal can only be in active state or inactive state and cannot be activated or deactivated.

Claim 10, line 5, "has been activated." should be changed to --is in the active state.-- for the similar reason as discussed in claim 9.

Claim 11, line 2, "at least one of" should be deleted because it does not make any sense for the transmission gate to be switched by an inverter controlled by the reset signal.

Claim 15, line 4, "loop a with" should be changed to --loop with--.

Claim 15, line 5, "signal, non-inverted" should be changed to --signal, the non-inverted-- to avoid unclear antecedent basis (see lines 2-3).

Claim 15, line 13, "the propagation delay" should be changed to --a propagation delay-- because this propagation delay is for the delay of the signal transferring from the second node to the inverted output node, i.e., it is not for the delay from the first node to the non-inverted output node.

Claims 16-20 are objected to because they include the informality of claim 15.

Also claim 18, line 1, "16" should be changed to --17-- to avoid lack antecedent basis since "the one or more gates of the second feedback loop" is recited in claim 17 (not claim 16).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 10 and 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 10, the recitation "and to apply a logic "0" to the fourth node in the second feedback loop when the reset signal has been activated" on the last 2 lines of the claim is indefinite since it is not clear how the decoupling circuit could apply a logic "0" to the fourth node in the second feedback loop. Note that, in operation of the circuit in Figure 8, it is seen that the decoupling circuit (20, 21) cannot apply a logic "0" to the fourth node (K4); and it is seen

that only the first feedback loop is capable of applying a logic "0" to the first node (K1) when the reset signal (R) is in the active state (i.e., when R = 0, then /R = 1 then K1 = 0). Therefore, to avoid the above problem and for claim 10 to be clear, it is suggested "and to apply a logic "0" to the fourth node in the second feedback loop when the reset signal has been activated" on the last 2 lines of the claim to be changed to --when the reset signal is in the active state, and wherein the first feedback loop applies a logic "0" to the first node when the reset signal is in the active state.--

With respect to claim 16, the recitation "the first feedback loop comprises a NOR gate" on line 1-2 cause the claim to be indefinite because it is not clear whether the first feedback loop further comprises a NOR in addition to the reset circuitry of the first feedback loop. It is seen that the claim should be recited that reset circuitry of the first feedback loop comprises a NOR gate rather than the first feedback loop comprises a NOR gate as currently recited in the claim. It appears that "wherein the first feedback" on line 1 of the claim should be changed to --wherein the reset circuitry of the first feedback--. Clarification and/or appropriate correction is requested.

With respect to claim 17, the recitation "the second feedback loop comprises one or more gates" on line 1-2 cause the claim to be indefinite because it is not clear whether the second feedback loop further comprises one or more gates in addition to the reset circuitry of the second feedback loop. It is seen that the claim should be recited that the reset circuitry of the second feedback loop comprises one or more gates rather than the second feedback loop comprises one or more gates as currently recited in the claim. It appears that "wherein the second" on line 1 of the claim should be changed to --wherein the reset circuitry of the second--. Clarification and/or appropriate correction is requested.

Claim 18 appears to be depended on claim 17 as discussed in the above claim objection, so claim 18 is indefinite for including the indefiniteness of claim 17. Further, the recitation "and an output cross-coupled with a NAND gate, wherein the NOR gate" on the last 2 lines of the claim is indefinite because the claim is incomplete and it is also unclear antecedent basis for "a NAND gate" in the above phrase. It appears that "and an output cross-coupled with a NAND gate, wherein the NOR gate" on the last 2 lines should be changed to –and an output coupled with the fourth node and the second input of the NOR gate--. Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 5, 9, 15, 16, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ichioka et al. (JP 2-210907).

With respect to claim 5, Figure 7 of the Ichioka et al. reference discloses a flip-flop which includes: a clock signal (CK); a data signal (D/); a non-inverted output (Q/); and inverted output (Q); a first holding element (51B, 52) having first (N42) and second (N41) nodes; and a second holding element (81, 82B) having third (N61) and fourth (N62) nodes; wherein the first node (N42) is coupled to the fourth node (N62) via a first signal path (N42→N52→N62) and the second node (N41) is coupled to the third node (N61) via a second signal path (N41→N51→N61) exclusive of the first signal path. Note that when clock CK = Hi (first level),

then the first node (N42) having the logic value of the data signal (D/) while the second node (N41) having the logic level of inverted logic value of the data signal (i.e., D); and when clock CK = Lo (second level), then the logic value (D/) at the first node (N42) is transferred and inverted to the fourth node (N62), and the inverted logic value (i.e., D) of the data signal (D/) at the second node (N41) is transferred and inverted to the third node (N61); wherein the fourth node (N62) corresponding the non-inverted output (Q/) and the third node (N61) corresponding to the inverted output (Q). Note that the second feedback look (81, 82B) comprises a NOR gate (81) responsive to reset signal (R).

With respect to claim 9, Figure 7 shows the first feedback loop (51B, 52) includes a NOR gate (52) so that the second node (N41) carries a logic "1" upon activation of the reset signal (i.e., when R = 1 then node N41 = 1).

With respect to claims 15-16, Figure 7 of the Ichioka et al. reference discloses a flip-flop which includes: a clock signal (CK); a data signal (D); a non-inverted output (Q); and inverted output (Q/); a first holding element (51B, 52) having first (N41) and second (N42) nodes; and a second holding element (81, 82B) having third (N62) and fourth (N61) nodes. Note that when clock CK goes Hi (first edge), then the first node (N41) having the logic value of the data signal (D) while the second node (N42) having the logic level of inverted logic value of the data signal (i.e., D/); and when clock CK goes Lo (second edge), then the logic value (D) at the first node (N41) is transferred to the non-inverted output node (Q) via the fourth node (N61), and the inverted logic value (i.e., D/) of the data signal (D) at the second node (N42) is transferred to the inverted output node (Q/) via the third node (N62). Note, it is seen in the operation of the flip-flop in Figure 7 that a propagation delay of the non-inverted logic level from the first node (N41)

to the non-inverted output node (Q) is substantially equal to a propagation delay of the inverted logic level from the second node (N42) to the inverted output node (Q/), i.e., each propagation delay = 2 inverters and 1 pass gate; and the first and second feedback loops each comprises reset circuitry (NOR gate 52 for the first feedback loop, and NOR gate 81 of second feedback loop) responsive to reset signal to the place the inverted and non-inverted output nodes at known logic levels regardless of the state of the clock signal (CK). Note that, the reset circuitry of the first feedback loop (i.e., NOR 52) comprises a NOR gate (52) having a first input coupled to R, a second input coupled to the second node N42, and an output coupled to the first node (N41).

With respect to claim 19, it is seen in Figure 7 that a first signal path between the first node (N41) and the non-inverted output node (Q) and a second signal path between the second node (N42) and the inverted output node (Q/) each comprises the same number of circuit elements (2 inverters and 1 pass gate).

With respect to claim 20, Figure 7 shows the first and second signal paths each comprises two inverters (61 and 91 for the first path, and 62 and 92 for the second path).

8. Claims 15-17 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Robertson et al. (US 2002/0005745 A1).

With respect to claims 15-16, Figure 11 of the Robertson et al. reference discloses a flip-flop which includes: a clock signal (CLK); a data signal (D); a non-inverted output (Q); and inverted output (QZ); a first holding element (39) having first (output of inverter 28) and second (input of inverter 28) nodes; and a second holding element (41) having third (input of inverter 31) and fourth (output of inverter 31) nodes. Note that when clock CLK goes Lo (first edge), then the first node having the logic value of the data signal (D) while the second node having the

logic level of inverted logic value of the data signal (i.e., D/); and when clock CLK goes Hi (second edge), then the logic value (D) at the first node is transferred to the non-inverted output node (Q) via the fourth node, and the inverted logic value (i.e., D/) of the data signal (D) at the second node (N42) is transferred to the inverted output node (QZ) via the third node. Note, it is seen in the operation of the flip-flop in Figure 11 that a propagation delay of the non-inverted logic level from the first node to the non-inverted output node (Q) is substantially equal to a propagation delay of the inverted logic level from the second node to the inverted output node (QZ), i.e., each propagation delay = 2 inverters and 1 pass gate; and the first and second feedback loops each comprises reset circuitry (NOR gate 40 for the first feedback loop, and NAND gate 42 of second feedback loop) responsive to reset signal (PREZ) to the place the inverted and non-inverted output nodes at known logic levels regardless of the state of the clock signal (CLK). Note that, the reset circuitry of the first feedback loop (i.e., NOR 40) comprises a NOR gate (40) having a first input coupled to signal PRE, a second input coupled to the second node (by way of inverter 28) and an output coupled to the first node (by way of inverter 28).

Insofar as understood in claim 17, Figure 11 shows the reset circuitry (NAND 42) of the second feedback loop (41) comprises one gate (42) controlled by the clock signal (CLK) and responsive to the reset signal (PREZ).

With respect to claim 19, it is seen in Figure 11 that a first signal path between the first node (output of 28) and the non-inverted output node (Q) and a second signal path between the second node (input of 28) and the inverted output node (QZ) each comprises the same number of circuit elements (2 inverters and 1 pass gate).

With respect to claim 20, Figure 11 shows the first and second signal paths each comprises two inverters (31 and 14 for the first path, and 28 and 25 for the second path).

Allowable Subject Matter

9. Claims 1-4 are presently allowed.

10. Claims 6-8, 10, 11 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if amended to overcome the informalities and/or the rejection under 35 U.S.C. 112, 2nd paragraph set forth above.

Response to Arguments

11. Applicant's arguments filed on 6/13/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 24, 2005

LONG NGUYEN
PRIMARY EXAMINER